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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,337	09/11/2003	Hitoshi Haematsu	020721A	7094

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EXAMINER	
PERKINS, PAMELA E	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 05/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/659,337	HAEMATSU, HITOSHI	
	Examiner	Art Unit	
	Pamela E Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 11 September 2003.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-3 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-3 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 11 September 2003 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/156,955.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the application papers on 11 September 2003. Claims 1-3 are pending.

Drawings

Figures 8A to 8E should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Tanimura (6,703,683).

Tanimura discloses a manufacturing method of a semiconductor device where a plurality electrodes (21,31) are formed front face of a semiconductor chip (1); covering

the front face of the semiconductor chip with a resin insulating film (52); covering all of an upper surface and side surfaces the resin insulating film (52) with a metal protective film (53) (Fig. 9, col. 7, lines 11-27); exposing one of the plurality of electrodes (21,31) from the upper surface the resin insulating film (52) to be connected to the metal protective film (53); and providing an electrical connecting portion (25,35) of at least any the plurality of electrodes (21,31) at a reverse face of the semiconductor chip (1) (col. 12, lines 12-65). Tanimura further discloses forming a metal layer (23,33) on a peripheral isolation region the front face the semiconductor chip (1) when covering the side surface of the resin insulating film (52) with the metal protective film (53) (col. 5, lines 26-43).

Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by Sugaya et al. (6,538,210).

Sugaya et al. discloses a manufacturing method of a semiconductor device where a plurality electrodes (211) are formed front face of a semiconductor chip; covering the front face of the semiconductor chip with a resin insulating film (200); covering all of an upper surface and side surfaces the resin insulating film (200) with a metal protective film (206); exposing one of the plurality of electrodes (211) from the upper surface the resin insulating film (200) to be connected to the metal protective film (206); and providing an electrical connecting portion (208) of at least any the plurality of electrodes (211) at a reverse face of the semiconductor chip (col. 13, line 14 thru col. 14, line 64).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nagano (5,357,056) discloses a manufacturing method of a semiconductor device where a plurality electrodes are formed front face of a semiconductor chip; covering the front face of the semiconductor chip with a resin insulating film; covering the resin insulating film with a metal protective film; and providing an electrical connecting portion of at least any the plurality of electrodes at a reverse face of the semiconductor chip. Takeuchi et al. (6,005,474) disclose a manufacturing method of a semiconductor device where a plurality electrodes are formed front face of a semiconductor chip; covering the front face of the semiconductor chip with a resin insulating film; covering the resin insulating film with a metal protective film; exposing one of the plurality of electrodes from the upper surface the resin insulating film to be connected to the metal protective film; and providing an electrical connecting portion of at least any the plurality of electrodes at a reverse face of the semiconductor chip.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP

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